



PCM1719

Sound PLUS™ Stereo Audio DIGITAL-TO-ANALOG CONVERTER

FEATURES

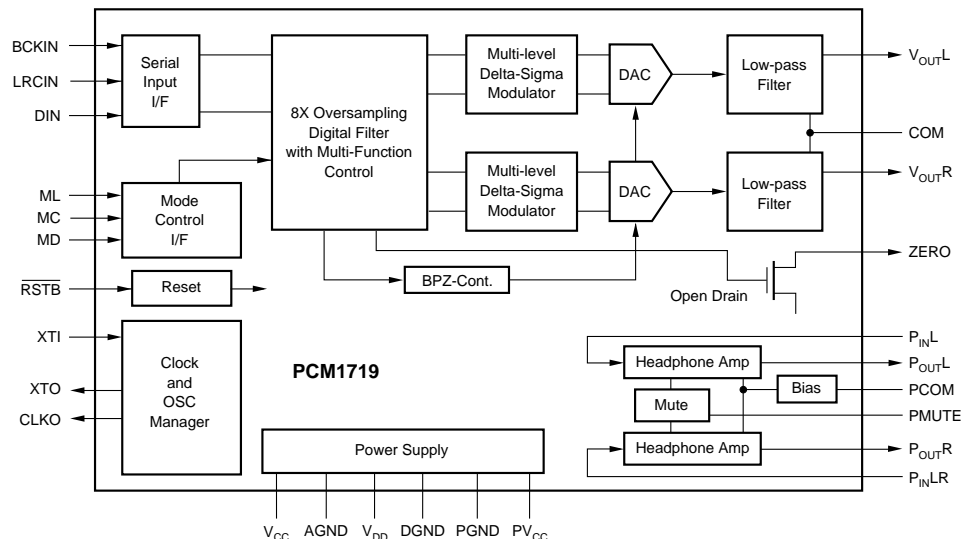
- ACCEPTS 16- OR 18-BIT INPUT DATA
- COMPLETE STEREO DAC:
 - 8X Oversampling Digital Filter
 - Multi-Level Delta-Sigma DAC
 - Analog Low Pass Filter
- ON-CHIP HEADPHONE AMPLIFIER
- HIGH PERFORMANCE:
 - 88dB THD+N
 - 96dB Dynamic Range
 - 100dB SNR
- SELECTABLE FUNCTIONS:
 - Digital De-emphasis
 - Digital Attenuation (256 Steps)
 - Soft Mute
 - Multiple Output Formats
- SYSTEM CLOCK: 256f_S or 384f_S
- SINGLE +5V POWER SUPPLY
- SMALL 28-PIN SSOP PACKAGE

DESCRIPTION

PCM1719 is a complete, low cost stereo audio digital-to-analog converter (DAC) including a digital interpolation filter, 3rd-order delta-sigma DAC, an analog low-pass filter and output amplifier. PCM1719 also has an on-chip stereo headphone amplifier.

PCM1719 can accept either 16-, or 18-bit input data. The audio data input format can be either MSB-first, right-justified or I²S. The system clock can be 256f_S or 384f_S. PCM1719 is fabricated on a highly advanced 0.6μs CMOS process, which delivers high performance at very low power dissipation.

PCM1719 is ideal for applications which require headphone drivers such as CD-ROM drives, digital audio workstations, portable CD players, and digital musical instruments.



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SPECIFICATIONS

All specifications at +25°C, +V_{DD} = +V_{CC} = PV_{CC} = +5V, f_S = 44.1kHz, SYSCLK = 384f_S, 16-bit data, unless otherwise noted.

| PARAMETER | CONDITIONS | PCM1719E | | | UNITS |
|---|---------------------------------------|--------------|------------------------------------|---------------|----------|
| | | MIN | TYP | MAX | |
| RESOLUTION | | 16 | | 18 | Bits |
| DATA FORMAT | | | | | |
| Audio Data Format | | | Normal/I ² S Selectable | | |
| Data Bit Length | | | 16/18 Bits, Selectable | | |
| Sampling Frequency (f _S) | 256f _S /384f _S | 32 | 44.1 | 48 | kHz |
| System Clock Frequency | | 8.192/12.288 | 11.2896/16.9344 | 12.288/18.432 | MHz |
| DIGITAL INPUT/OUTPUT | | | | | |
| Logic Family | | | TTL Compatible | | |
| Input Logic Level ^{(2), (3)} | | | | | |
| V _{IH} | | 2 | | | VDC |
| V _{IL} | | | | 0.8 | VDC |
| Input Logic Current | | | | | |
| I _{IH} | | | | 0.8 | μA |
| I _{IL} | | | | -0.8 | μA |
| I _{IH} | V _{IH} = 2.0V | | | -100 | μA |
| I _{IL} | V _{IL} = 0.0V | | | -120 | μA |
| I _{IH} | V _{IH} = 2.0V | | | 15 | μA |
| I _{IL} | V _{IL} = 0.0V | | | -15 | μA |
| I _{IH} | V _{IH} = 2.0V | | | -60 | μA |
| I _{IL} | V _{IL} = 0.0V | | | -100 | μA |
| Output Logic Level | | | | | |
| V _{OH} | I _{OH} = -5mA | 3.8 | | | VDC |
| V _{OL} | I _{OL} = 5mA | | | 1.0 | VDC |
| V _{OL} | I _{OL} = 5mA | | | 1.0 | VDC |
| DYNAMIC PERFORMANCE⁽¹⁾ | | | | | |
| V_{OUTL}, V_{OUTR}: Line Output⁽⁵⁾ | | | | | |
| THD+N at V _O = 0dB | f _{OUT} = 991Hz | | -88 | -80 | dB |
| at V _O = -60dB | f _{OUT} = 991Hz | | -34 | | dB |
| Dynamic Range | EIAJ, A-weighted | 90 | 96 | | dB |
| Signal-to-Noise Ratio | EIAJ, A-weighted | 92 | 100 | | dB |
| Channel Separation | f _{OUT} = 991Hz | 90 | 97 | | dB |
| Level Linearity Error | f _{OUT} = 991Hz, -90dB | | ±0.5 | | dB |
| P_{OUTL}, P_{OUTR}: Headphone Output⁽⁶⁾ | R _L = 64Ω | | | | |
| THD+N at V _O = 0dB | | | -68 | -60 | dB |
| Frequency Response | f _{OUT} = 20Hz to 20kHz | | ±0.1 | ±0.2 | dB |
| Output Noise Level | EIAJ, A-weighted, R _G = 0Ω | | 25 | 30 | μVrms |
| Channel Separation | | 87 | 90 | | dB |
| Analog Mute Attenuation Level | | 80 | 85 | | dB |
| DC PERFORMANCE | | | | | |
| V_{OUTL}, V_{OUTR}: Line Output⁽⁵⁾ | | | | | |
| Gain Error | R _L = 64Ω | | ±1 | ±5 | % of FSR |
| Gain Mismatch Channel-to-Channel | | | ±1 | ±5 | % of FSR |
| Bipolar Zero Error | V _{OUT} = V _{CC} /2 | | ±30 | | mV |
| Analog Output Range | | | 3.1 | | Vp-p |
| Center Voltage | | | V _{CC} /2 | | V |
| AC Load Impedance | | | 50% of V _{CC} | | VDC |
| P_{OUTL}, P_{OUTR}: Headphone Output⁽⁶⁾ | | | | | |
| Voltage Gain | Load = 64Ω | 5 | -2.8 | | dB |
| Voltage Gain Error | G = -2.8dB | | ±0.1 | ±0.2 | dB |
| Input Offset Voltage | Load = 64Ω | | ±30 | | mV |
| Gain Mismatch Channel-to-Channel | Load = 64Ω | | ±0.1 | ±0.2 | dB |
| Maximum Output Current | | | 12.5 | | mArms |
| Maximum Output Voltage | | | 0.8 | | Vrms |
| Output Power | | | 10 | | mW |
| AC Load Impedance | | | 64 | | Ω |

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SPECIFICATIONS(Cont)

All specifications at +25°C, +V_{DD} = +V_{CC} = PV_{CC} = +5V, f_S = 44.1kHz, SYSCLK = 384f_S, 16-bit data, unless otherwise noted.

| PARAMETER | CONDITIONS | PCM1719E | | | UNITS |
|------------------------------------|--|----------|-----------------------|-------|----------------|
| | | MIN | TYP | MAX | |
| FILTER PERFORMANCE | | | | | |
| Digital Filter | | | | | |
| Passband | | | | 0.445 | f _S |
| Stopband | | 0.555 | | | f _S |
| Passband Ripple | | | | ±0.17 | dB |
| Stopband Attenuation | | -35 | | | dB |
| De-emphasis Error | | -0.2 | | +0.55 | dB |
| Delay Time | f _S = 32kHz to 48kHz | | 11.125/f _S | | sec |
| ANALOG FILTER: Line Outputs | | | | | |
| Frequency Response | f = 20Hz to 20kHz | | -0.16 | | dB |
| POWER SUPPLY REQUIREMENTS | | | | | |
| Voltage Range | V _{DD} , V _{CC} , PV _{CC} | +4.5 | 5.0 | +5.5 | VDC |
| Supply Current ⁽⁷⁾ | | | 18 | 25 | mA |
| I _{CC} + I _{DD} | V _{DD} = V _{CC} = 5.0V | | 18 | 25 | mA |
| I _{CC} (Full Scale Input) | PV _{CC} = 5.0V | | 20 | 25 | mA |
| Power Dissipation | | | | | |
| P _D | V _{CC} , V _{DD} = 5.0 | | 90 | 125 | mW |
| P _{PD} | PV _{CC} = 5.0 | | 90 | 125 | mW |
| TEMPERATURE RANGE | | | | | |
| Operation | | -25 | | +85 | °C |
| Storage | | -55 | | +100 | °C |

NOTES: (1) Dynamic performance specs are tested with external 20kHz low pass filter and THD-B specs are test with 30kHz LPF, 400Jz HPF, Average Mode, Shibasoku #725 THD Meter. (2) RSTB pin, MD pin, MC pin, and ML pin include an internal pull-up resistor. (3) RSTB pin, MD pin, MC pin, and ML pin include internal Schmitt trigger circuits. (4) ZERO pin is an open drain output. (5) Line output should be connected by a coupling capacitor. (6) Headphone output should be connected by a coupling capacitor. (7) Supply current and power dissipation are measured at CLK0 pin = no load, XTO pin = no load.

ABSOLUTE MAXIMUM RATINGS

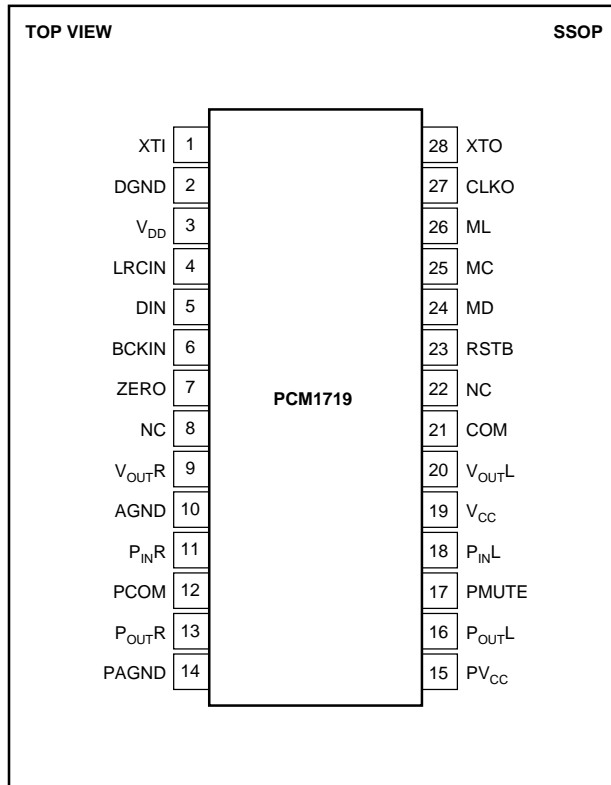
| | |
|---|----------------------------------|
| Power Supply Voltage | |
| +V _{DD} | +6.5V |
| +V _{CC} | +6.5V |
| +PV _{CC} | +6.5V |
| -V _{DD} to +V _{CC} Δ | 0.1V |
| +V _{DD} to +PV _{CC} Δ | 0.1V |
| +V _{DD} to +PV _{CC} Δ | 0.1V |
| Input Logic Voltage | -0.6V to (V _{DD} + 06V) |
| Power Dissipation | 200mW |
| Operating Temperature Range | -25°C to +85°C |
| Storage Temperature | -55°C to +125°C |
| Lead Temperature (soldering, 5s) | +260°C |
| Junction Temperature, θ _{JA} | +130°C/W |

PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER ⁽¹⁾ |
|----------|-------------|---------------------------------------|
| PCM1719E | 28-Pin SSOP | 324 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

PIN CONFIGURATION



PIN ASSIGNMENTS

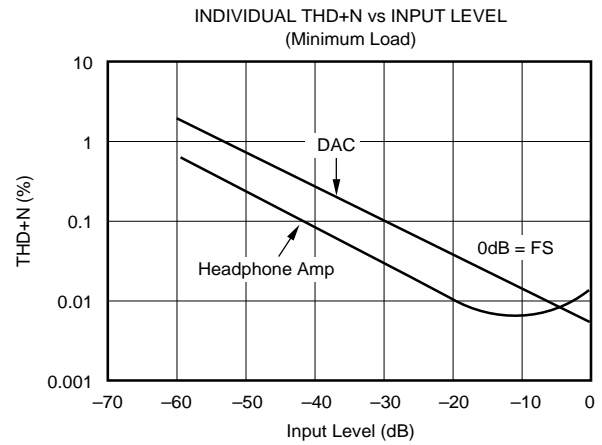
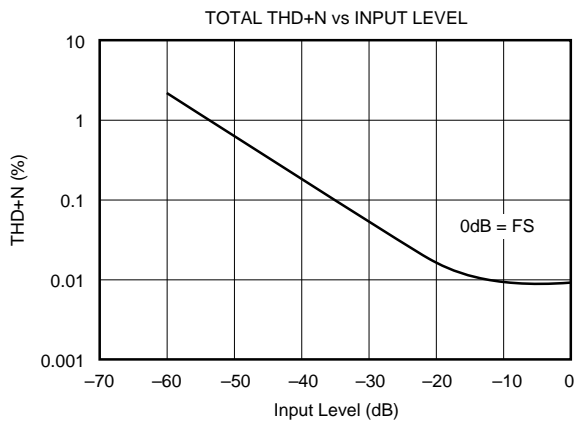
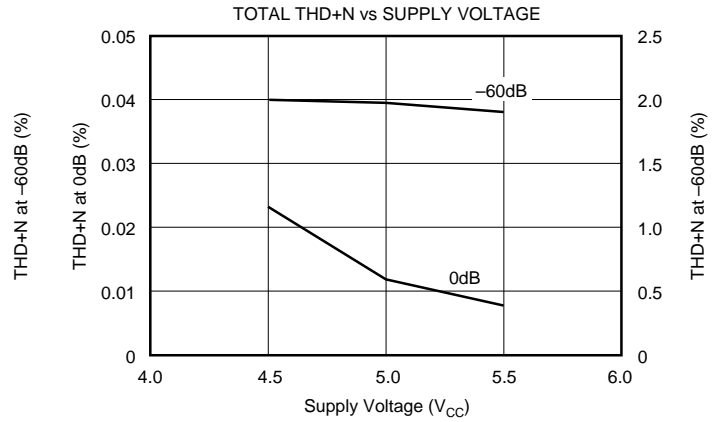
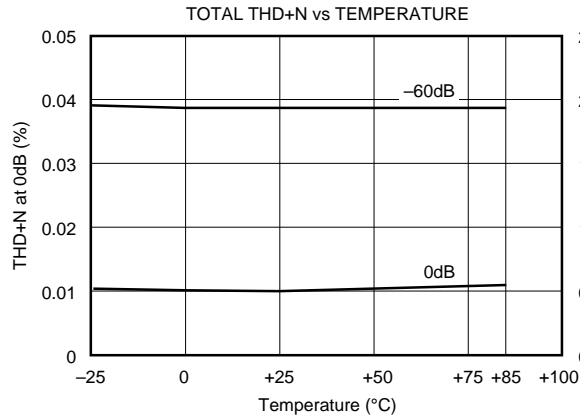
| PIN | NAME | TYPE | FUNCTION |
|-------------------|-------------------|------|--|
| 1 | XTI | IN | Crystal Oscillator Input. |
| 2 | DGND | PWR | Digital Ground. |
| 3 | V _{DD} | PWR | +5V Digital Power Supply. |
| 4 ⁽¹⁾ | LRCIN | IN | Left/Right Word Clock. Frequency is equal to f _s . |
| 5 | DIN | IN | Serial Audio Data Input. |
| 6 | BCKIN | IN | Bit Clock for Loading in Audio Data. |
| 7 | ZERO | OUT | Zero Data Flag. This pin is "LOW" when the input data is continuously zero for 65, 536 periods of BCKIN. |
| 8 | NC | — | No Connection. |
| 9 | V _{OUTR} | OUT | Right-Channel Analog Line Output. |
| 10 | AGND | PWR | Analog Ground. |
| 11 | P _{INR} | IN | Input for Headphone Amplifier, Right-Channel. |
| 12 | PCOM | PWR | Headphone Amplifier Common. Bypass with 100μF. |
| 13 | P _{OUTR} | OUT | Right-Channel Headphone Amplifier Output. |
| 14 | PAGND | PWR | Headphone Amplifier Ground. |
| 15 | PVCC | PWR | +5V Headphone Amplifier Power Supply. |
| 16 | P _{OUTL} | OUT | Left-Channel Headphone Amplifier Output. |
| 17 ⁽¹⁾ | PMUTE | IN | Mute Control for Headphone Amplifier. |
| 18 | P _{INL} | IN | Input for Headphone Amplifier, Left-Channel. |
| 19 | V _{CC} | PWR | +5V Analog Power Supply. |
| 20 | V _{OUTL} | OUT | Left-Channel Analog Line Output. |
| 21 | COM | PWR | Line Out Common. Bypass with 10μF. |
| 22 | NC | — | No Connection. |
| 23 ⁽¹⁾ | RSTB | IN | External Reset Control. |
| 24 ⁽¹⁾ | MD | IN | Data for Serial Control. |
| 25 ⁽¹⁾ | MC | IN | Clock for Serial Control. |
| 26 ⁽¹⁾ | ML | IN | Latch for Serial Control. |
| 27 | CLKO | OUT | System Clock (256f _s or 384f _s) Output. |
| 28 | XTO | OUT | Crystal Oscillator Output. |

NOTE: (1) With internal pull-up.

TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, $V_{CC} = V_{DD} = PV_{CC} = +5\text{V}$, $R_L = 32\Omega + 32\Omega$, and $f = 1\text{kHz}$, $384f_s$, unless otherwise noted.

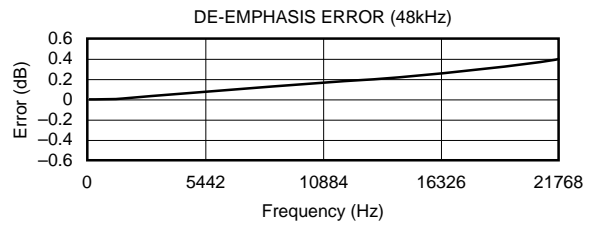
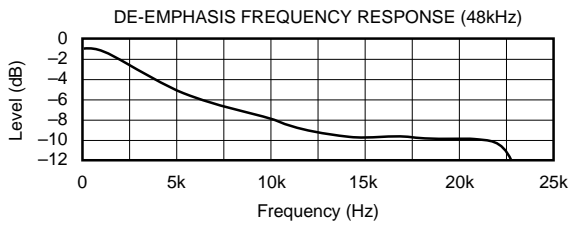
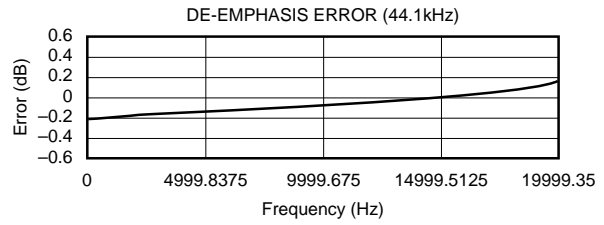
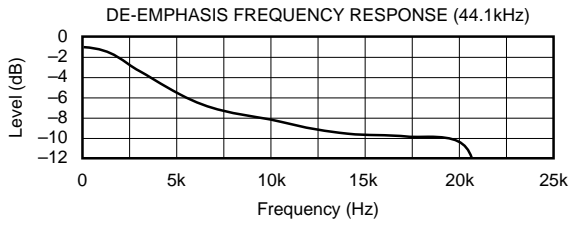
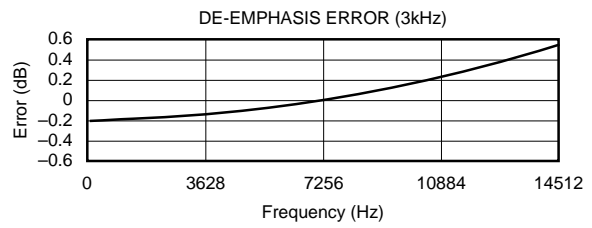
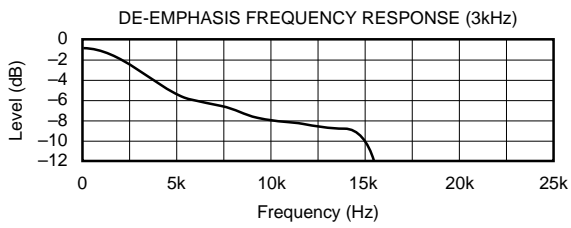
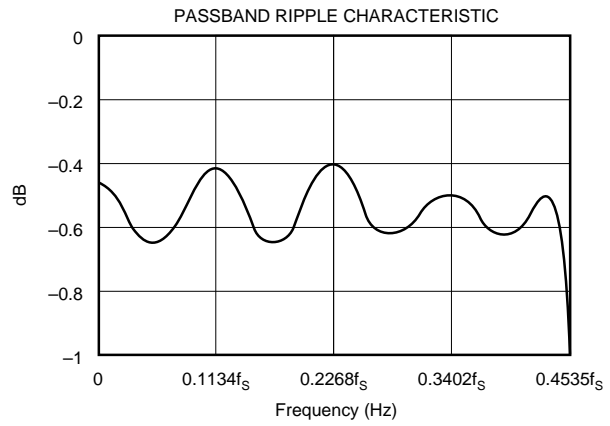
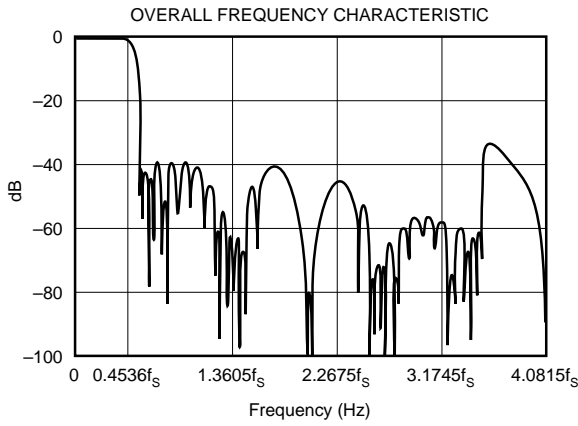
ANALOG PERFORMANCE



TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, $V_{CC} = V_{DD} = PV_{CC} = +5\text{V}$, $R_L = 64\Omega$, $f_{SYS} = 384f_S$, and 16-bit input data, unless otherwise noted.

DIGITAL FILTER



SYSTEM CLOCK

The system clock of PCM1719 must be either $256f_s$ or $384f_s$, where f_s is the audio sampling frequency, such as 32kHz, 44.1kHz, and 48kHz. The system clock is used to operate the digital filter and the multi-level delta-sigma modulator. The system clock can be either a crystal oscillator placed across XTI (pin 1) and XTO (pin28), or an external clock input to the XTI pin directly. In this case, the XTO pin should be open (floating). Figure 1 illustrates the internal clock circuit and typical connection.

The PCM1719 has a system clock detection circuit which automatically detects the system clock of either $256f_s$ or $384f_s$. The system clock should be synchronized with the LRCIN (pin 4) clock (sampling frequency), but the PCM1719 allows for a phase difference between LRCIN and the system clock. If the phase difference between LRCIN and system clock is larger than ± 6 bit clocks (BCKIN), the synchronization of the system clock and LRCIN is done

automatically. The analog outputs are forced to $V_{CC}/2$ during the synchronization operation. Table I shows the system clock frequency input to the PCM1719.

| SAMPLING RATE FREQUENCY (LRCIN) | SYSTEM CLOCK FREQUENCY (MHz) | |
|------------------------------------|---------------------------------|----------|
| | $256f_s$ | $384f_s$ |
| 32kHz | 8.1920 | 12.2880 |
| 44.1kHz | 11.2896 | 16.9340 |
| 48kHz | 12.2880 | 18.4320 |

TABLE I. System Clock Frequencies vs Sampling Rate.

INFINITE ZERO FLAG FUNCTION

When the audio input data (at both channels) is continuously zero (BPZ code) for 65, 536 cycles of bit clock (BCKIN), ZERO (pin 7) goes to a "LOW" level. When the audio input data is non-zero, the ZERO pin goes to a high-impedance state immediately. This pin is open-drain.

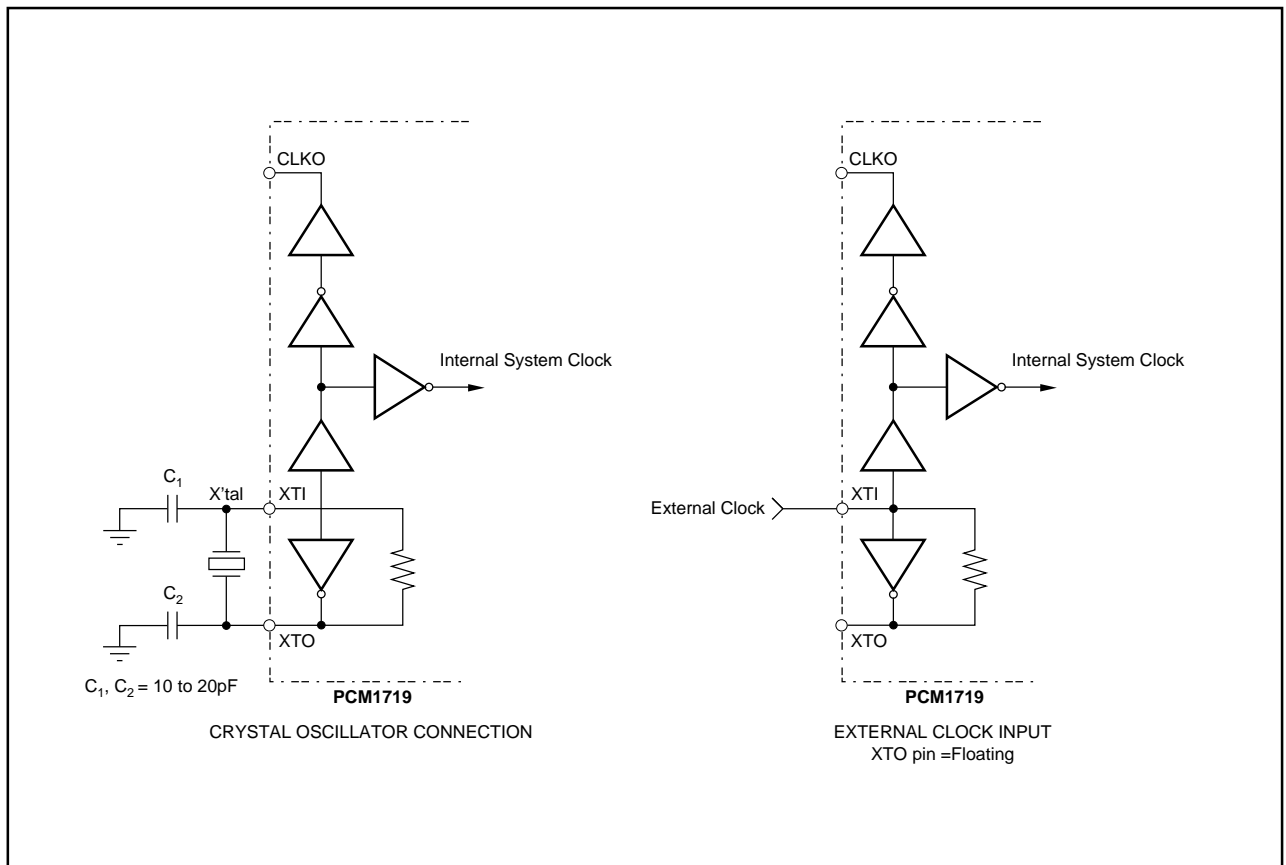


FIGURE 1. Internal Clock Circuit Diagram and Oscillator Connection.

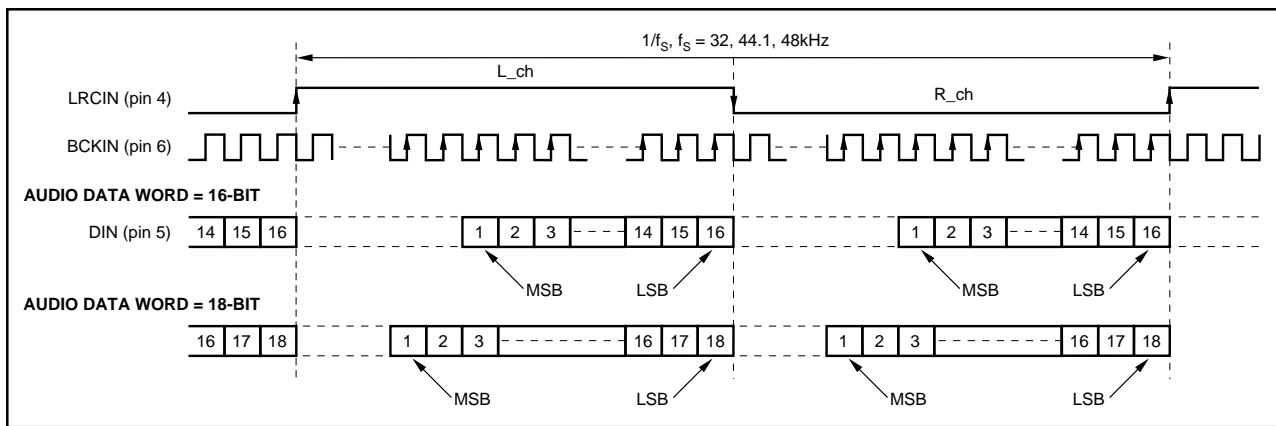


FIGURE 2. Data Input Timing of Normal Format (MSB-first, right-justified); Lch = “H”, Rch = “L”.

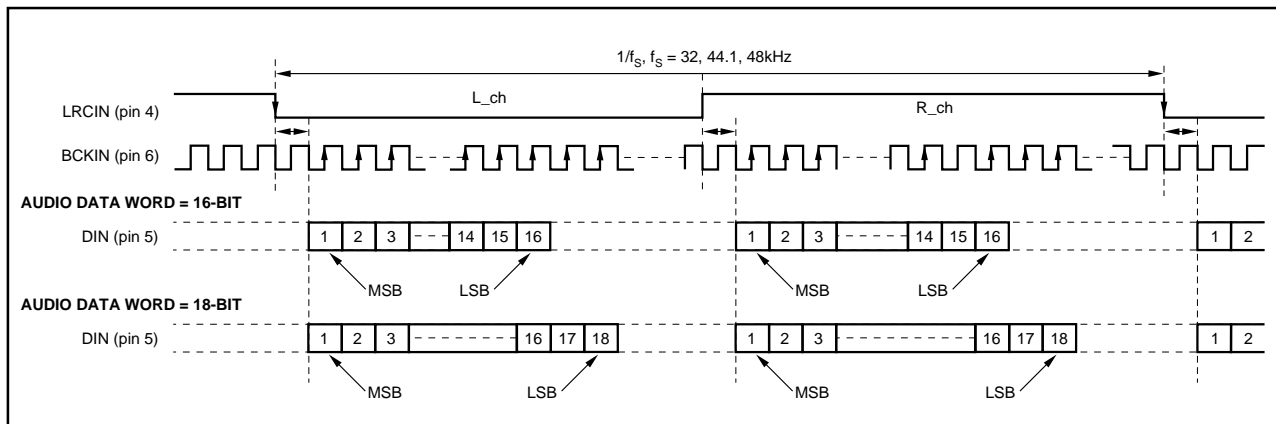


FIGURE 3. Data Input Timing of I²S Data Format (Philips format); Lch = “L”, Rch = “H”.

PCM AUDIO INTERFACE

PCM audio data of the PCM1719 is accepted via LRCIN (pin 4), DIN (pin 5) and BCKIN (pin 6). The PCM1719E accepts both normal and I²S data input formats. The normal data format is MSB-first, Two’s Complement and right-justified. The I²S format is compatible with Philips’ serial data protocol. In these formats, the serial data is 16- or 18-bit input selectable. Figures 2 and 3 illustrate the input audio data timing and format.

OPERATIONAL CONTROL

The Software Mode uses a three-wire interface on pins 24, 25 and 26. Pin 25 (MC) is used to clock in the serial control data, pin 26 (ML) is used to latch the serial control data, and pin 24 (MD) is used to load in the serial control register. There are four distinct registers, with bits 9 and 10 (of 16) determining which register is in use.

REGISTER CONTROL (Bits 9, 10)

| REGISTER | B9 (A0) | B10 (A1) |
|----------|---------|----------|
| 0 | 0 | 0 |
| 1 | 1 | 0 |
| 2 | 0 | 1 |
| 3 | 1 | 1 |

Control data timing is shown in Figure 7. ML is used to latch the data from the control registers. After each register’s contents are checked in, ML should be taken “LOW” to latch in the data. A “res” in the register indicates that location is reserved for factory use. When loading the registers, the “res” bits should be set “LOW”.

REGISTER 0

| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-----|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| res | res | res | res | res | A1 | A0 | LDL | AL7 | AL6 | AL5 | AL4 | AL3 | AL2 | AL1 | AL0 |

Register 0 is used to control left channel attenuation. Bits 0-7 (AL0-AL7) are used to determine the attenuation level. The level of attenuation is given by:

$$ATT = [20\log_{10} (ATT_DATA/255)] \text{ dB}$$

ATTENUATION DATA LOAD CONTROL, LCH

Bit 8 (LDL) is used to simultaneously set analog outputs of Lch and Rch. An output level is controlled by AL[0:7] attenuation data when this bit is set to 1. When set to 0, an output level is not controlled and remained at the previous attenuation level. A LDR bit in Register 1 has an equivalent function as the LDL. When one of LDL or LDR is set to 1, the output level of the left and right channel is simultaneously controlled. The attenuation level is given by:

$$ATT = 20 \log (y/256) \text{ (dB)}, \text{ where } y = x, \text{ when } 0 \leq x \leq 254$$

$$y = x + 1, \text{ when } x = 255$$

X is the user-determined step number, an integer value between 0 and 255.

Example:

let $x = 255$

$$ATT = 20 \log \left(\frac{255+1}{256} \right) = 0 \text{ dB}$$

let $x = 254$

$$ATT = 20 \log \left(\frac{254}{256} \right) = -0.068 \text{ dB}$$

let $x = 1$

$$ATT = 20 \log \left(\frac{1}{256} \right) = -48.16 \text{ dB}$$

let $x = 0$

$$ATT = 20 \log \left(\frac{0}{256} \right) = -\infty$$

REGISTER 1

Register 1 is used to control right channel attenuation. As in Register 1, bits 0-7 (AR0-AR7) control the level of attenuation.

| | | | | | | | | | | | | | | | |
|-----|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| res | res | res | res | res | A1 | A0 | LDR | AR7 | AR6 | AR5 | AR4 | AR3 | AR2 | AR1 | AR0 |

REGISTER 2

| | | | | | | | | | | | | | | | |
|-----|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|-----|-----|-----|------|
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| res | res | res | res | res | A1 | A0 | res | res | res | res | IZD | OPE | DM1 | DM0 | MUTE |

Register 2 is used to control soft mute, digital de-emphasis, disable, and infinite zero detect. Bit 0 is used for soft mute; a HIGH level on bit 0 will cause the output to be muted. Bits 1 and 2 are used to control digital de-emphasis as shown below:

| BIT 1 (DM0) | BIT 2 (DM1) | DE-EMPHASIS |
|-------------|-------------|--------------------------------|
| 0 | 0 | De-emphasis disabled |
| 1 | 0 | De-emphasis enabled at 48kHz |
| 0 | 1 | De-emphasis enabled at 44.1kHz |
| 1 | 1 | De-emphasis enabled at 32kHz |

Bits 3 (OPE) and 4 (IZD) are used to control the infinite zero detection features. Tables II through IV illustrate the relationship between IZD, OPE, and RSTB (reset control):

| | DATA INPUT | DAC OUTPUT |
|---------|------------|------------------------------|
| IZD = 1 | Zero | Forced to BPZ ⁽¹⁾ |
| | Other | Normal |
| IZD = 0 | Zero | Zero ⁽²⁾ |
| | Other | Normal |

TABLE II. Infinite Zero Detection (IZD) Function.

| | DATA INPUT | DAC OUTPUT | SOFTWARE MODE INPUT |
|---------|------------|------------------------------|---------------------|
| OPE = 1 | Zero | Forced to BPZ ⁽¹⁾ | Enabled |
| | Other | Forced to BPZ ⁽¹⁾ | Enabled |
| OPE = 0 | Zero | Controlled by IZD | Enabled |
| | Other | Normal | Enabled |

TABLE III. Output Enable (OPE) Function.

| | DATA INPUT | DAC OUTPUT | SOFTWARE MODE INPUT |
|---------------|------------|------------------------------|---------------------|
| RSTB = "HIGH" | Zero | Controlled by OPE and IZD | Enabled |
| | Other | Controlled by OPE and IZD | Enabled |
| RSTB = "LOW" | Zero | Forced to BPZ ⁽¹⁾ | Disabled |
| | Other | Forced to BPZ ⁽¹⁾ | Disabled |

TABLE IV. Reset (RSTB) Function.

NOTE: (1) $\Delta\Sigma$ is disconnected from output amplifier. (2) $\Delta\Sigma$ is connected to output amplifier.

OPE controls the operation of the DAC: when OPE is "LOW", the DAC will convert all non-zero input data. If the input data is continuously zero for 65,536 cycles of BCKIN, the output will only be forced to zero only if IZD is "HIGH". When OPE is "HIGH", the output of the DAC will be forced to bipolar zero, irrespective of any input data.

IZD controls the operation of the zero detect feature: when IZD is "LOW", the zero detect circuit is off. Under this condition, no automatic muting will occur if the input is continuously zero. When IZD is "HIGH", the zero detect feature is enabled. If the input data is continuously zero for 65,536 cycles of BCKIN, the output will be immediately forced to a bipolar zero state ($V_{CC}/2$). The zero detection feature is used to avoid noise which may occur when the input is DC. When the output is forced to bipolar zero, there may be an audible click. PCM1719 allows the zero detect feature to be disabled so the user can implement an external muting circuit.

REGISTER 3

| | | | | | | | | | | | | | | | |
|-----|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|-----|----|-----|-----|
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| res | res | res | res | res | A1 | A0 | res | PL3 | PL2 | PL1 | PL0 | ATC | IW | LRP | IIS |

Register 3 is used to select the I/O data formats. Bit 0 (IIS) is used to control the input data format. If the input data source is normal (16- or 18-bit, MSB first, right-justified), set bit 0 "LOW". If the input format is I²S, set bit 0 "HIGH".

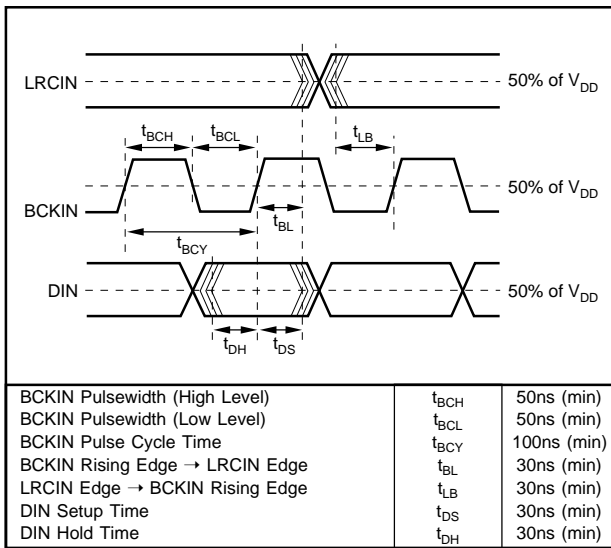


FIGURE 4. Data Input Timing.

Bit 1 is used to select the polarity of LRCIN (sample rate clock). When bit 1 is LOW, a HIGH state on LRCIN is used for the left channel, and a LOW state on LRCIN is used for the right channel. When bit 1 is HIGH the polarity of LRCIN is reversed.

Bit 2 is used to select the input word length. When bit 2 is LOW, the input word length is set for 16 bits; when bit 2 is HIGH, the input word length is set for 18 bits.

Bit 3 is used as an attenuation control. When bit 3 is set HIGH, the attenuation data on Register 0 is used for both channels, and the data in Register 1 is ignored. When bit 3 is LOW, each channel has separate attenuation data.

Bits 4 through 7 are used to determine the output format, as shown in Table V:

| PL0 | PL1 | PL2 | PL3 | Lch OUTPUT | Rch OUTPUT | NOTE |
|-----|-----|-----|-----|------------|------------|---------|
| 0 | 0 | 0 | 0 | MUTE | MUTE | MUTE |
| 0 | 0 | 0 | 1 | MUTE | R | |
| 0 | 0 | 1 | 0 | MUTE | L | |
| 0 | 0 | 1 | 1 | MUTE | (L + R)/2 | |
| 0 | 1 | 0 | 0 | R | MUTE | |
| 0 | 1 | 0 | 1 | R | R | |
| 0 | 1 | 1 | 0 | R | L | REVERSE |
| 0 | 1 | 1 | 1 | R | (L + R)/2 | |
| 1 | 0 | 0 | 0 | L | MUTE | |
| 1 | 0 | 0 | 1 | L | R | STEREO |
| 1 | 0 | 1 | 0 | L | L | |
| 1 | 0 | 1 | 1 | L | (L + R)/2 | |
| 1 | 1 | 0 | 0 | (L + R)/2 | MUTE | |
| 1 | 1 | 0 | 1 | (L + R)/2 | R | |
| 1 | 1 | 1 | 0 | (L + R)/2 | L | |
| 1 | 1 | 1 | 1 | (L + R)/2 | (L + R)/2 | MONO |

TABLE V. PCM1719 Output Mode Control.

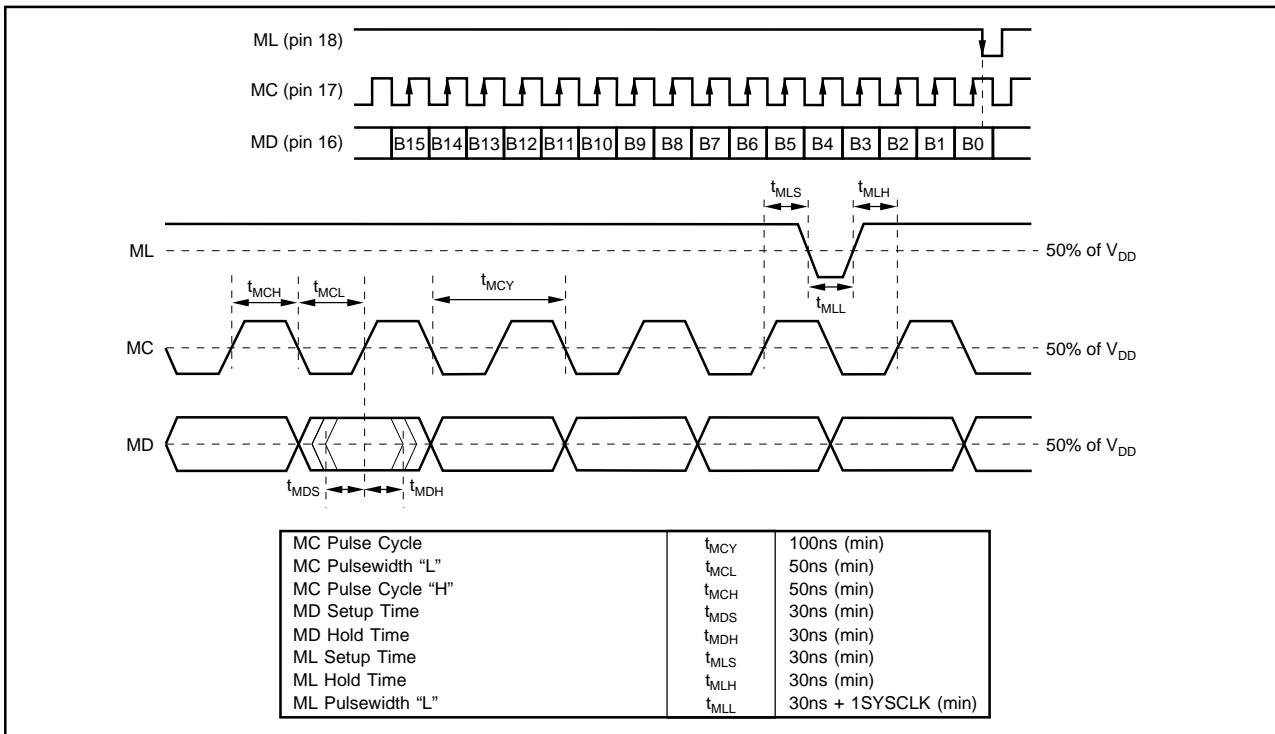


FIGURE 5. Control Data Timing in Software Mode Control.

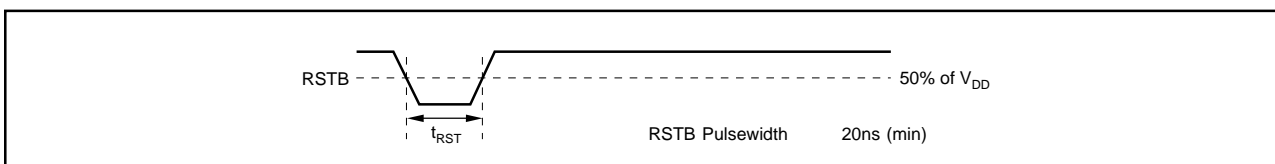


FIGURE 6. External Reset Timing.

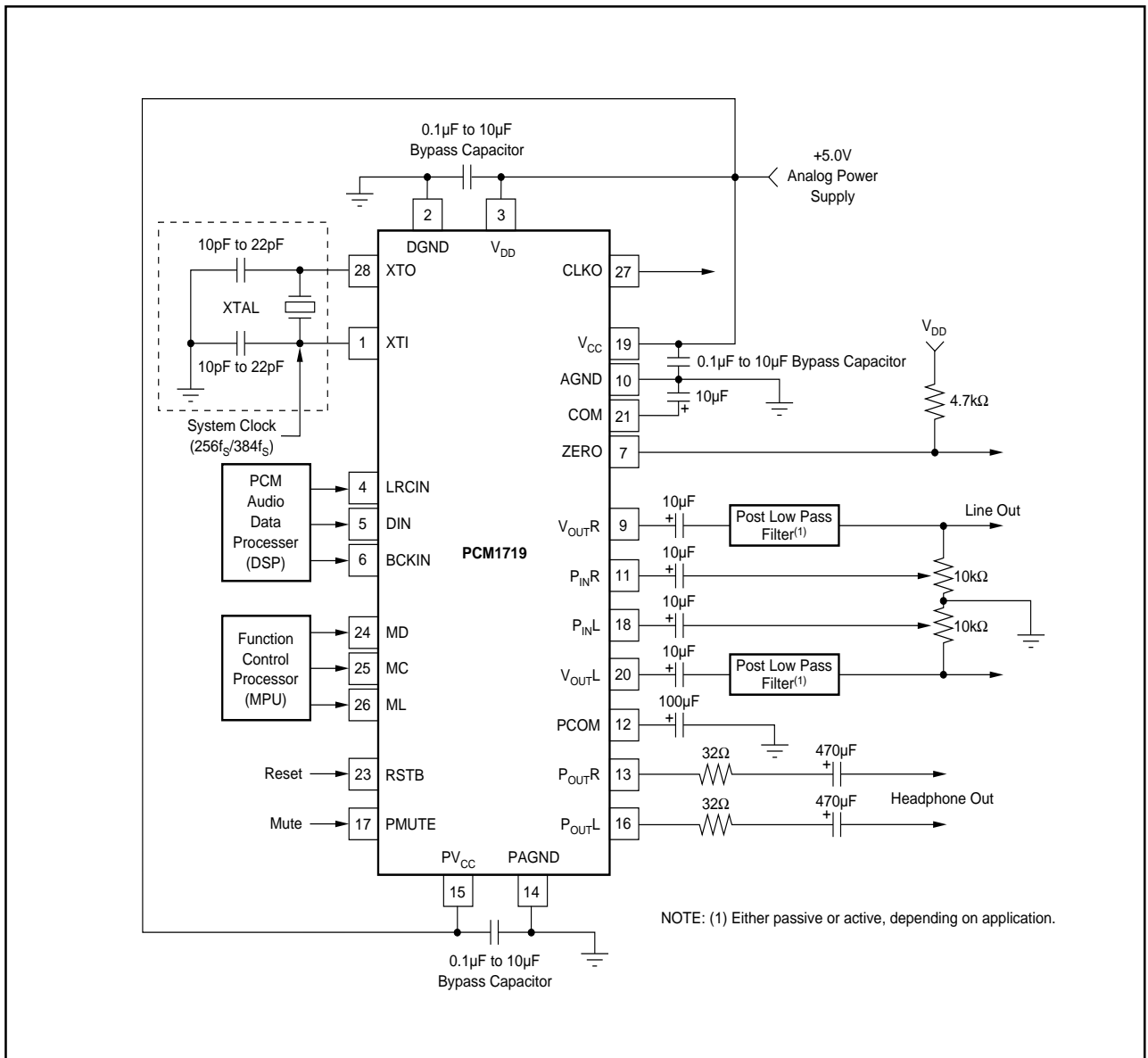


FIGURE 7. Typical Circuit Connection.

TYPICAL APPLICATION CIRCUIT

Figure 7 shows the typical application circuit. In this circuit, V_{DD} , V_{CC} , and PV_{CC} are connected to a common analog power supply. It is possible to use separate analog and digital power supplies for PCM1719. If separate supplies are used, the difference voltage between the supplies must be less than $\pm 0.1V$. PCM1719's headphone amplifier allows for high current flow from the outputs to ground. To keep the high load current from affecting the DAC's performance, the headphone jack ground should be connected to a low-impedance ground plane. Interference from the headphone amplifier can also be minimized by using a separate power supply for PV_{CC} , but avoid power supply deltas greater than $\pm 0.1V$.

Bypassing and decoupling capacitors should be placed as close as possible to the device pin. The capacitance between PCOM (pin 12) and/or COM (pin 21) to ground can be reduced to $1\mu F$, but this may decrease performance of the PCM1719's internal analog low-pass filter. The $10\mu F$ capacitor shown between COM and analog ground is used to set the pole for the PCM1719's internal low-pass filter. It is also important to limit the measurement bandwidth of the PCM1719 to 20kHz during performance evaluation. By definition, delta-sigma DACs have a large amount of energy beyond the audio band. Including this energy in THD+N measurements will not demonstrate the true in-band performance of PCM1719.

POWER SUPPLY CONNECTIONS

PCM1719 has two power supply connections: digital (V_{DD}) and analog (V_{CC}). Each connection also has a separate ground. If the power supplies turn on at different times, there is a possibility of a latch-up condition. To avoid this condition, it is recommended to have a common connection between the digital and analog power supplies. If separate supplies are used without a common connection, the delta between the two supplies during ramp-up time must be less than 0.6V.

An application circuit to avoid a latch-up condition is shown in Figure 8.

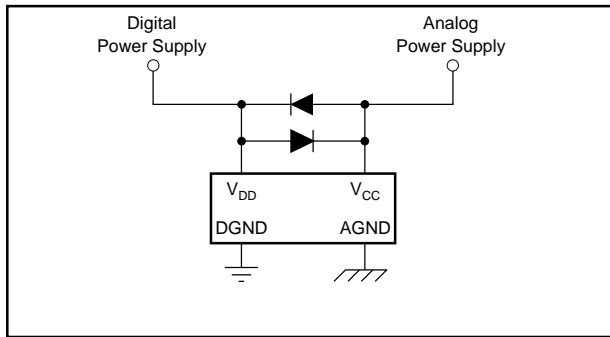


FIGURE 8. Latch-up Prevention Circuit.

THEORY OF OPERATION

The delta-sigma section of PCM1719 is based on a 5-level amplitude quantizer and a 3rd-order noise shaper. This section converts the oversampled input data to 5-level delta-sigma format.

A block diagram of the 5-level delta-sigma modulator is shown in Figure 9. This 5-level delta-sigma modulator has the advantage of stability and clock jitter sensitivity over the typical one-bit (2 level) delta-sigma modulator.

The combined oversampling rate of the delta-sigma modulator and the internal 8-times interpolation filter is $48f_s$ for a $384f_s$ system clock, and $64f_s$ for a $256f_s$ system clock. The theoretical quantization noise performance of the 5-level delta-sigma modulator is shown in Figure 10.

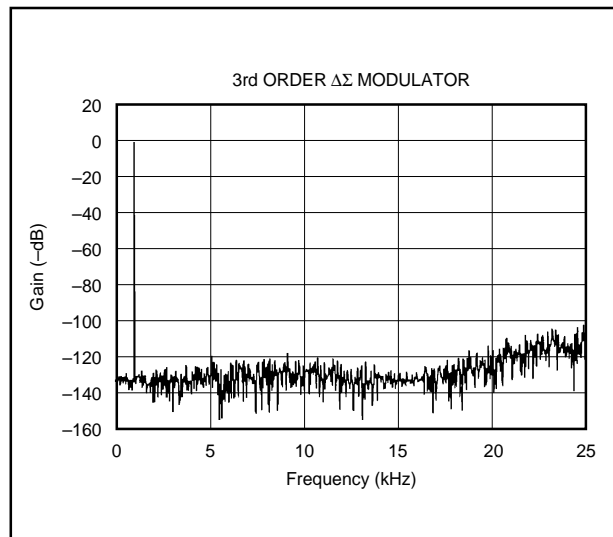


FIGURE 10. Quantization Noise Spectrum.

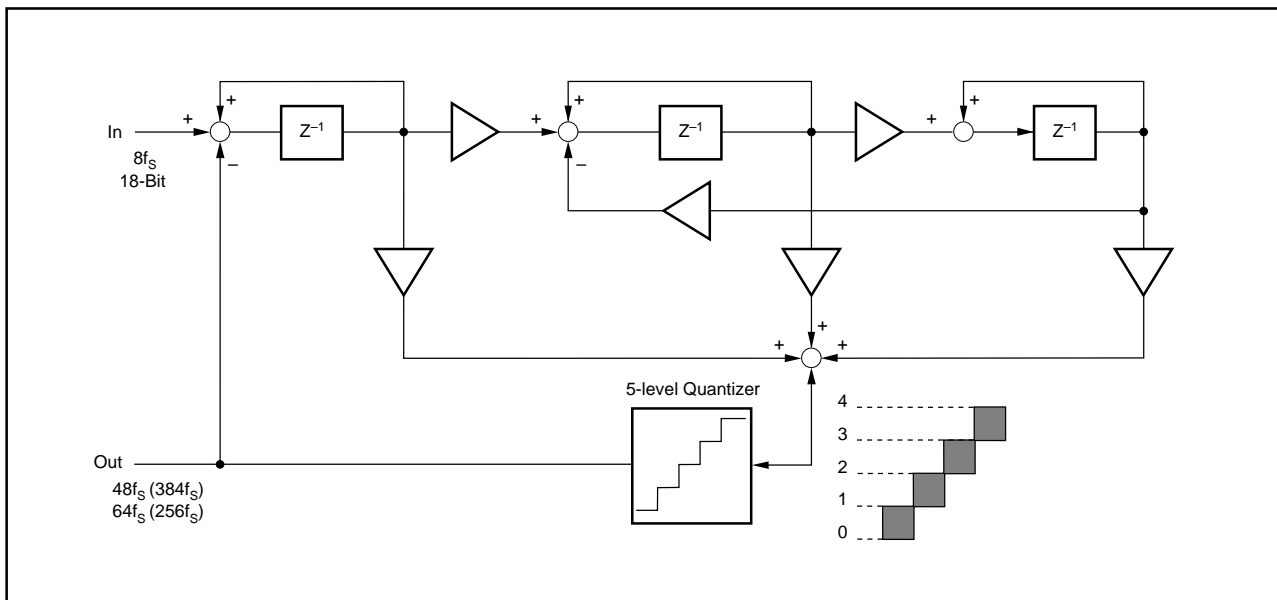


FIGURE 9. 5-Level $\Delta\Sigma$ Modulator Block Diagram.

APPLICATION CONSIDERATIONS

DELAY TIME

There is a finite delay time in delta-sigma converters. In A/D converters, this is commonly referred to as latency. For a delta-sigma D/A converter, delay time is determined by the order number of the FIR filter stage, and the chosen sampling rate. The following equation expresses the delay time of PCM1719:

$$T_D = 11.125 \times 1/f_S$$

For $f_S = 44.1\text{kHz}$, $T_D = 11.125/44.1\text{kHz} = 502.8\mu\text{s}$

Applications using data from a disc or tape source, such as CD audio, CD-Interactive, Video CD, DAT, Minidisc, etc., generally are not affected by delay time. For some professional applications such as broadcast audio for studios, it is important for total delay time to be less than 2ms.

INTERNAL RESET

When power is first applied to PCM1719, an automatic reset function occurs after 1,024 cycles of XTI clock. Refer to Table I for default conditions. During the first 1,024 cycles of XTI clock, PCM1719 cannot be programmed (Software Control). Data can be loaded into the control registers during this time, and after 1,204 cycles of XTI clock, a "LOW" on ML (pin 18) will initiate programming.

OUTPUT FILTERING

For testing purposes all dynamic tests are done on the PCM1719 using a 20kHz low pass filter. This filter limits the measured bandwidth for THD+N, etc. to 20kHz. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the specifications. The low pass filter removes out-of-band noise. Although it is not audible, it may affect dynamic specification numbers.

The performance of the internal low pass filter from DC to 24kHz is shown in Figure 11. The higher frequency rolloff of the filter is shown in Figure 12. If the user's application has the PCM1719 driving a wideband amplifier, it is recommended to use an external low pass filter. A simple 3rd-order filter is shown in Figure 13. For some applications, a passive RC filter or 2nd-order filter may be adequate.

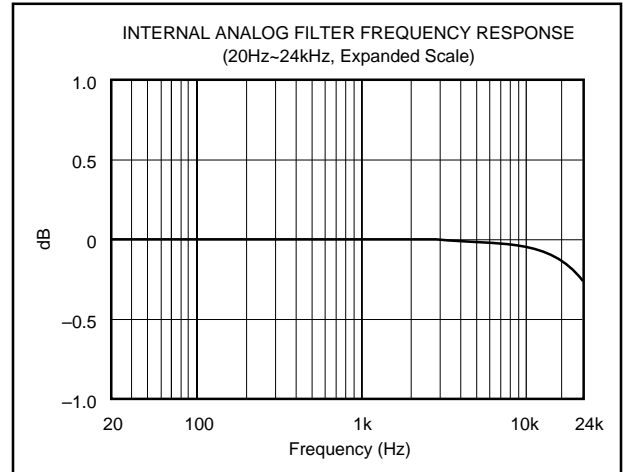


FIGURE 11. Low Pass Filter Frequency Response.

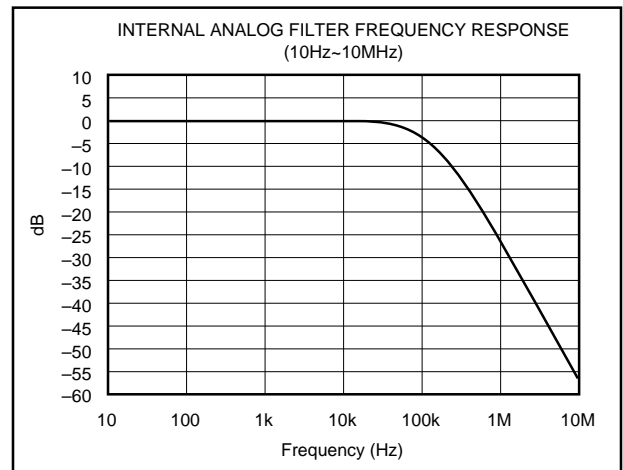


FIGURE 12. Low Pass Filter Frequency Response.

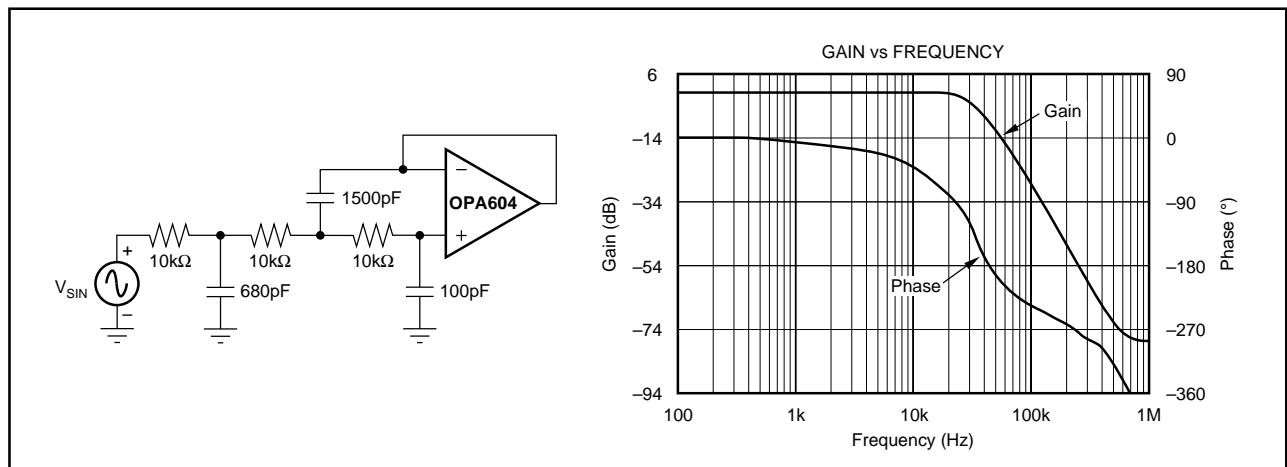


FIGURE 13. 3rd-Order LPF.

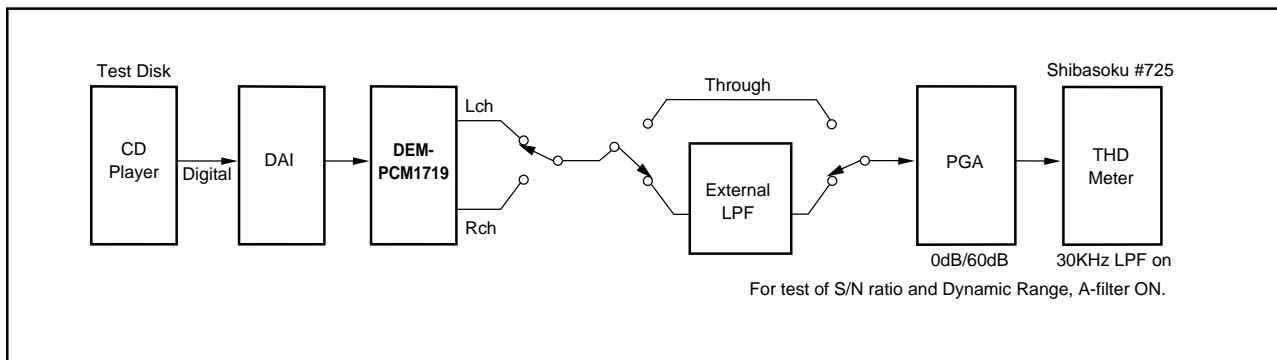


FIGURE 14. Test Block Diagram.

TEST CONDITIONS

Figure 14 illustrates the actual test conditions applied to PCM1719 in production. The external filter is necessary in the production environment for the removal of noise resulting from the relatively long physical distance between the unit and the test analyzer. In most actual applications, the 3rd-order filter shown in Figure 13 is adequate. Under normal conditions, THD+N typical performance is -70dB with a 30kHz low pass filter (shown here on the THD meter), improving to -89dB when the external 20kHz 11th-order filter is used.

JITTER SENSITIVITY

Delta-sigma DACs are by nature very sensitive to jitter on the master clock. Phase noise on the clock will result in an increase in noise, ultimately degrading dynamic range. It is difficult to quantify the effect of jitter due to problems in synthesizing low levels of jitter. One of the reasons delta-sigma DACs are prone to jitter sensitivity is the large quantization noise when the modulator can only achieve two discrete output levels (0 or 1). The multi-level delta-sigma DAC has improved theoretical SNR because of multiple output states. This reduces sensitivity to jitter. Figure 15 contrasts jitter sensitivity between a one-bit PWM type DAC and multi-level delta-sigma DAC. The data was derived using a simulator, where clock jitter could be completely synthesized.

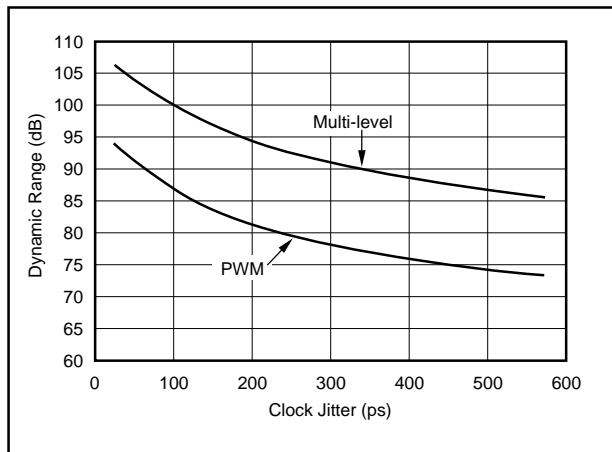


FIGURE 15. Simulation Results of Clock Jitter Sensitivity.

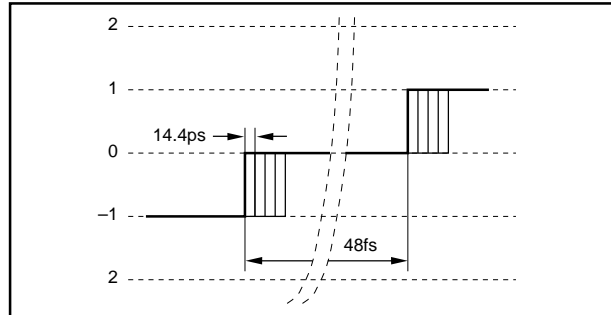


FIGURE 16. Simulation Method for Clock Jitter.

HEADPHONE AMPLIFIER

PCM1719 has an integrated headphone amplifier which can directly drive a 32Ω load, such as headphones. The amplifier is configured in a gain of -2.8dB (inverting), and the maximum output current is 12.5mA (rms). The maximum output voltage is 0.8Vrms into a 64Ω load (stereo 32Ω headphones), based on the typical DAC full scale output of 3.1V (p-p). P_{IN}L and P_{IN}R should be AC-coupled such that the input impedance for the headphone amplifier is 55kΩ typical, and the noninverting input is biased to V_{CC}/2.

The headphone amplifier has no internal current limiting circuit. It is recommended to use an external current limiting resistor to avoid damage caused by overloading the output, and avoid shorting P_{OUT}L and P_{OUT}R to ground. The minimum output load of 64Ω includes any current limiting resistor. If the input impedance of the headphone is 32Ω, a current limiting resistor of 32Ω should be used. Figure 17

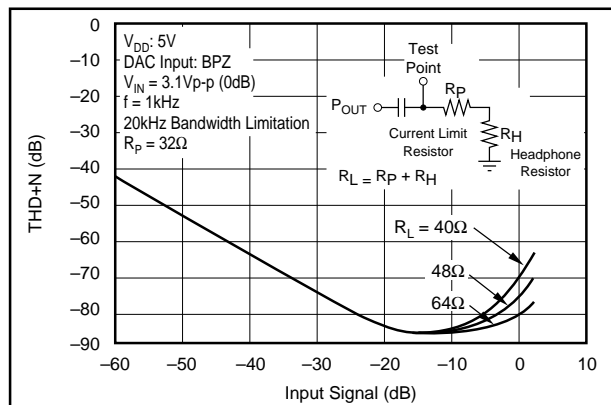


FIGURE 17. THD+N vs Input Signal, Output Load.

illustrates THD+N versus input signal and output load. The PCM1719 headphone amplifier specification for THD+N is done with a 64Ω load at 12.5mA (rms) maximum output current. Although PCM1719 is capable of driving loads as low as 15Ω , the output waveform will be saturated under such a condition. The recommended application circuit employs a 32Ω load with a 32Ω current limiting resistor.

VOLUME CONTROL

PCM1719 allows the user to attenuate the volume by using a variable resistor. In the actual application, a $10k\Omega$ pot is connected between the line (DAC) outputs and analog ground,

with the center tap of the pot AC-coupled to the headphone amplifier's inputs. Refer to Figure 7, the typical connection diagram, for an illustration of this circuit.

ANALOG MUTE FUNCTION

The headphone amplifier's output can be muted to -80dB . When PMUTE is taken "LOW", the headphone outputs are muted. For normal operation, PMUTE should be held "HIGH" or left open.